IN THE CLAIMS:

Rewrite the pending claims as follows:

1 – 14 (Cancelled)

15. (Previously presented) A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench, said first gate region continuous in a lateral direction parallel to said surface;

implanting a buffer region beneath said first gate region; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region, and wherein, at a conclusion of implanting said second gate region, said second gate region is continuous in said lateral direction and is narrower than said first gate region.

16. (Previously presented) The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said first gate region.

17. (Original) The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said buffer region.

18. (Previously presented) The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said second gate region.

19. (Previously presented) The method of Claim 15, further comprising annealing said substrate subsequent to implanting said second gate region.

20. (Previously presented) The method of Claim 15, further comprising annealing said substrate after said implanting said second gate region.

21. (Previously presented) A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

in sequence,

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench;

implanting a buffer region beneath said first gate region; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region; wherein said first gate region and said second gate region together form said dual gate structure.

22. (Previously presented) The method of Claim 21, further comprising forming a sidewall spacer to establish a width of said first gate region.

23. (Previously presented) The method of Claim 21, further comprising forming a sidewall spacer to establish a width of said buffer region.

24. (Previously presented) The method of Claim 21, further comprising forming a sidewall spacer to establish a width of said second gate region.

25. (Previously presented) The method of Claim 21, wherein said first gate region is continuous in a lateral direction parallel to said surface, and said second gate region is continuous in said lateral direction and is narrower than said first gate region.

26. (Previously presented) A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench;

after forming the first gate region, implanting a buffer region beneath said first gate region; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region; wherein said first gate region and said second gate region together form said dual gate structure.

27. (Previously presented) The method of Claim 26, further comprising forming a sidewall spacer to establish a width of said first gate region.

28. (Previously presented) The method of Claim 26, further comprising forming a sidewall spacer to establish a width of said buffer region.

29. (Previously presented) The method of Claim 26, further comprising forming a sidewall spacer to establish a width of said second gate region.

30. (Previously presented) A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench;

implanting a buffer region beneath said first gate region; and

after implanting the buffer region, implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region; wherein said first gate region and said second gate region together form said dual gate structure.

31. (Previously presented) The method of Claim 30, further comprising forming a sidewall spacer to establish a width of said first gate region.

32. (Previously presented) The method of Claim 30, further comprising forming a sidewall spacer to establish a width of said buffer region.

33. (Previously presented) The method of Claim 30, further comprising forming a sidewall spacer to establish a width of said second gate region.

34. (Previously presented) The method of Claim 30, further comprising forming a first sidewall spacer to establish a width of said buffer region, and forming a second sidewall spacer to establish a width of said second gate region, wherein the second sidewall spacer is thicker than the first sidewall spacer.